AMENDMENT TO THE CLAIMS:

This listing of claims will replace all prior versions of claims in the application:

LISTING OF CLAIMS:

1. (CURRENTLY AMENDED) A preamplifier system, comprising:

~~(a)~~ a magneto-resistive (MR) sensor;

~~(b)~~ an alternating current (AC) coupling module coupled to the MR sensor for blocking a direct current (DC) voltage associated with an input signal, and filtering low frequency noise associated with the input signal;

~~(c)~~ a gain stage module coupled to the AC coupling module, the gain stage module including a plurality of cascode field effect transistors (FETs) configured for amplifying the input signal, while reducing intrinsic noise and increasing operational bandwidth; ~~and~~

~~(d) a control circuit coupled to the gain stage module for feeding back an output of the gain stage module~~

wherein the gain stage module includes a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal, and a drain terminal coupled to the output of the gain stage module.

2. (CURRENTLY AMENDED) ~~The system as recited in claim 1~~ A preamplifer system, comprising:

a magneto-resistive (MR) sensor;

an alternating current (AC) coupling module coupled to the MR sensor for blocking a direct current (DC) voltage associated with an input signal, and filtering low frequency noise associated with the input signal;

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a gain stage module coupled to the AC coupling module, the gain stage module including a plurality of cascode field effect transistors (FETs) configured for amplifying the input signal, while reducing intrinsic noise and increasing operational bandwidth; and

a control circuit coupled to the gain stage module for feeding back an output of the gain stage module,

wherein one of the cascode FETs includes a dimension ratio (width/length) with a value of at least 4000.

3. (CURRENTLY AMENDED) ~~The system as recited in claim 1~~ A preamplifer system, comprising:

a magneto-resistive (MR) sensor;

an alternating current (AC) coupling module coupled to the MR sensor for blocking a direct current (DC) voltage associated with an input signal, and filtering low frequency noise associated with the input signal;

a gain stage module coupled to the AC coupling module, the gain stage module including a plurality of cascode field effect transistors (FETs) configured for amplifying the input signal, while reducing intrinsic noise and increasing operational bandwidth; and

a control circuit coupled to the gain stage module for feeding back an output of the gain stage module,

wherein the gain stage module includes a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal, and a drain terminal coupled to the output of the gain stage module; a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to the power source, and a drain terminal coupled to the power source; a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the

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drain terminal of the first transistor, and a drain terminal coupled to the gate terminal of the second transistor; a fifth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the drain terminal of the fourth transistor and the gate terminal of the second transistor; and a capacitor coupled between ground and the drain terminal of the fifth transistor, the drain terminal of the fourth transistor, and the gate terminal of the second transistor.

4. (ORIGINAL) The system as recited in claim 3, wherein the AC coupling module includes a capacitor including a first terminal coupled to the gate terminal of the first transistor and the MR sensor.

5. (ORIGINAL) The system as recited in claim 3, wherein the control circuit includes an operational transductance amplifier with a first input coupled to the output of the gain stage module and a second input coupled to a reference output, the operational transductance amplifier including an output coupled to a gate terminal of a sixth transistor including a source terminal coupled to the power source, and a drain terminal, the control circuit further including a first resistor having a first terminal coupled to the drain terminal of the sixth transistor and a second terminal coupled to the gate terminal of the first transistor, a second resistor including a first terminal coupled to the drain terminal of the sixth transistor and a second terminal coupled to ground.

6. (ORIGINAL) The system as recited in claim 5, wherein the reference output is defined by an eighth transistor including a source terminal, a gate terminal, and a drain terminal coupled to the reference output; a ninth transistor including a source terminal coupled to the reference output, a gate terminal coupled to the power source, and a drain terminal coupled to the power source; and a current

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source including a first terminal coupled to the source terminal of the eighth transistor and a second terminal coupled to ground.

7. (ORIGINAL) The system as recited in claim 3, wherein a gain at the drain terminal of the first transistor is less than one (1).

8. (CURRENTLY AMENDED) A preamplifying method, comprising:

~~(a)~~ receiving an input signal from a magneto-resistive (MR) sensor;

~~(b)~~ blocking a direct current (DC) voltage associated with the input signal;

~~(c)~~ filtering low frequency noise associated with the input signal;

~~(d)~~ amplifying the input signal utilizing a plurality of cascode field effect transistors (FETs)~~; and~~

~~(e) feeding back an output of the amplification utilizing a control circuit~~ including a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal, and a drain terminal coupled to the output of the gain stage module; a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to the power source, and a drain terminal coupled to the power source; a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the drain terminal of the first transistor, and a drain terminal coupled to the gate terminal of the second transistor.

9. (ORIGINAL) A preamplifier circuit, comprising:

a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal;

a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal, and a drain terminal coupled to an output;

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a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to the power source, and a drain terminal coupled to the power source;

a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the drain terminal of the first transistor, and a drain terminal coupled to the gate terminal of the second transistor;

a fifth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the gate terminal of the second transistor and the drain terminal of the fourth transistor; and

a capacitor coupled between ground and the drain terminal of the fifth transistor, the drain terminal of the fourth transistor, and the gate terminal of the second transistor.

10. (ORIGINAL) The preamplifier circuit as recited in claim 9, wherein the first transistor includes a field effect transistor (FET).

11. (ORIGINAL) The preamplifier circuit as recited in claim 10, wherein the first transistor includes a dimension ratio (width/length) with a value of at least 4000.

12. (ORIGINAL) The preamplifier circuit as recited in claim 9, and further comprising a sixth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal.

13. (ORIGINAL) The preamplifier circuit as recited in claim 12, and further comprising a seventh transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to a magneto-resistive (MR) sensor.

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14. (ORIGINAL) The preamplifier circuit as recited in claim 13, and further comprising an eighth transistor including a source terminal, a gate terminal, and a drain terminal coupled to a second output.

15. (ORIGINAL) The preamplifier circuit as recited in claim 14, and further comprising a ninth transistor including a source terminal coupled to the second output, a gate terminal coupled to the power source, and a drain terminal coupled to the power source.

16. (ORIGINAL) The preamplifier circuit as recited in claim 15, and further comprising an operational transductance amplifier with a first input coupled to the first output and a second input coupled to the second output, the operational transductance amplifier including an output coupled to the gate terminal of the sixth transistor.

17. (ORIGINAL) The preamplifier circuit as recited in claim 16, and further comprising a first current source including a first terminal coupled to the source terminal of the eighth transistor and a second terminal coupled to ground.

18. (ORIGINAL) The preamplifier circuit as recited in claim 17, and further comprising a second current source including a first terminal coupled to the power source and a second terminal coupled to the gate terminal of the fourth transistor.

19. (ORIGINAL) The preamplifier circuit as recited in claim 18, and further comprising another capacitor including a first terminal coupled to the gate terminal of the first transistor and a second terminal coupled to a magneto-resistive (MR) sensor.

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20. (ORIGINAL) A preamplifier circuit system, comprising:

a magneto-resistive (MR) sensor including a first terminal coupled to ground and a second terminal;

a first transistor including a source terminal coupled to ground, a gate terminal coupled to a first node, and a drain terminal;

a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal coupled to a second node, and a drain terminal coupled to a first output;

a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to a power source, and a drain terminal coupled to the power source;

a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the drain terminal of the first transistor, and a drain terminal coupled to the second node;

a fifth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the second node;

a sixth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to a third node;

a seventh transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the second terminal of the MR sensor;

an eighth transistor including a source terminal, a gate terminal, and a drain terminal coupled to a second output;

a ninth transistor including a source terminal coupled to the second output, a gate terminal coupled to the power source, and a drain terminal coupled to the power source;

an operational transductance amplifier with a first input coupled to the first output and a second input coupled to the second output, the operational transductance amplifier including an output coupled to the gate terminal of the sixth transistor;

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a first current source including a first terminal coupled to the source terminal of the eighth transistor and a second terminal coupled to ground;

a second current source including a first terminal coupled to the power source and a second terminal coupled to the gate terminal of the fourth transistor;

a first capacitor including a first terminal coupled to the power source and a second terminal coupled to the gate terminal of the sixth transistor;

a second capacitor including a first terminal coupled to the second node and a second terminal coupled to ground;

a third capacitor including a first terminal coupled to the first node and a second terminal coupled to the second terminal of the MR sensor;

a first resistor including a first terminal coupled to the third node and a second terminal coupled to the first node; and

a second resistor including a first terminal coupled to the third node and a second terminal coupled to ground.

21. (CURRENTLY AMENDED) A disk drive system, comprising:

a magnetic recording disk;

a magnetic head including an magneto-resistive (MR) sensor;

an actuator for moving the magnetic head across the magnetic recording disk so the magnetic head may access different regions of the magnetic recording disk; and

a controller electrically coupled to the magnetic head including a preamplifier including:

an alternating current (AC) coupling module coupled to the MR sensor for blocking a direct current (DC) voltage associated with an input signal, and filtering low frequency noise associated with the input signal,

a gain stage module coupled to the AC coupling module, the gain stage module including a plurality of cascode field effect transistors (FETs) configured for amplifying the input signal, while reducing intrinsic noise and increasing

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operational bandwidth, wherein the gain stage module includes a first transistor including a source terminal coupled to ground, a gate terminal, and a drain terminal; a second transistor including a source terminal coupled to the drain terminal of the first transistor, a gate terminal, and a drain terminal coupled to the output of the gain stage module; a third transistor including a source terminal coupled to the drain terminal of the second transistor, a gate terminal coupled to the power source, and a drain terminal coupled to the power source; a fourth transistor including a source terminal coupled to ground, a gate terminal coupled to the drain terminal of the first transistor, and a drain terminal coupled to the gate terminal of the second transistor; a fifth transistor including a source terminal coupled to the power source, a gate terminal, and a drain terminal coupled to the drain terminal of the fourth transistor and the gate terminal of the second transistor; and a capacitor coupled between ground and the drain terminal of the fifth transistor, the drain terminal of the fourth transistor, and the gate terminal of the second transistor, and

a control circuit coupled to the gain stage module for feeding back an output of the gain stage module.

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